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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,697	07/15/2003	Karen L. Noel	200312434-1	7142

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EXAMINER	
PATEL, KAUSHIKKUMAR M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,697	NOEL ET AL.	
	Examiner	Art Unit	
	Kaushikkumar Patel	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. This Office Action is in response to applicant's communication filed March 31, 2006 in response to PTO office action mailed February 2, 2006. The applicant's remarks with respect to claims were considered with the results that follow.

2. In response to last Office action, no claims have been amended. Claims 1-19 remain pending in this application.

3. Applicant's arguments with respect to claims 1, 8, 12 and 16 have been fully considered but they are not persuasive.

With respect to applicant's arguments regarding claim 1, Harvey teaches a multiprocessor system with each processor with associated memory (fig. 2) with a replicated versions of operating system and data. Harvey also teaches processing system using virtual memory. It is well known in the art that virtual memory management is handled by the operating system. With replicated versions of the operating system in each of the processing elements same (replicated) operating system handles the virtual to physical memory translation same way (i.e. same virtual address refers to same physical address (see Harvey column 2, lines 23-33). Harvey fails to teach mapping of virtual address to physical address (keeping page tables in respective memories) as per claim 1. But it is obvious to one having ordinary skill in the art to store page table in respective memories associated with individual processors and such virtual address refers to same physical address as explained in column 2, lines 23-33 of Harvey.

With respect claims 8, 12 and 16, applicant argues Harvey fails to teach read/write variables. According to definition from present application specification, paragraph [0002], the read/write variables means counters. (Counters are not explicitly defined further in the specification. With respect to that definition any counter is a read/write variable). de Backer (US 6,233,688 B1) teaches a counter as explained with respect to rejections of claim 3-7 in previous office action. Thus the combination of Harvey and de Backer teaches a read/write variable and multiprocessor system with replicated versions of operating system and data. Harvey and de Backer teach the importance of keeping data being local to processors (i.e. data in respective processor's memory). So it would have been obvious to one having ordinary skill in the art at the time of the invention to keep all the related data (page tables and other related data) in the local memories of the respective processors (see previous office action pages 3-4, with respect to rejection of claims 3-7). Claims 8-19 are also rejected under same rationales (combination of Harvey and de Backer) as applied to claims 1-7.

Due to reasons discussed above, the rejection of claims 1-19 are respectfully maintained and reiterated below.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harvey et al. (US 6,233,668 B1) (Harvey herein after).

Regarding claim 1, Harvey teaches a method of running multiprocessor system (fig. 2) with replicated data and operating systems on all the processing nodes (column 3, lines 37-40) using virtual memory address (VMA) (column 1, lines 44-60) and runs a instances of programs with their respective page tables (fig. 1). Harvey implicitly failed to teach claim 1, but it obvious to one having ordinary skill in the art at the time of the invention that, multiprocessor system (fig. 2) running replicated versions of data and operating systems (column 3, lines 37-40) can execute a first instance of a program (operating system) on a first processor (fig. 2, item 48) and second instance of the program on second processor (fig. 2, item 50) and maintain respective page tables in respective memories. Also since, system uses virtual memory addressing it also obvious that during execution of the instance of the program refers to memory address using page tables and pointers to refer to same physical memory address using VMA (column 2, lines 23-33).

Regarding claim 2, Harvey teaches that data and operating system program is replicated in individual memories of the processor to reduce the cost of the non-uniform access times (column 3, lines 37-40), thus Harvey teaches a functional unit with replicated versions of the same program running respective instances of the programs.

Claim Rejections - 35 USC § 103

6. Claims 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harvey et al. (US 6,233,688 B1) as applied to claims 1 and 2 above, and further in view of de Backer et al. (US 6,266,745 B1) (Backer herein after).

Harvey teaches a method of multiprocessor system running replicated versions of data and operating system as applied to claims 1 and 2 above, but fails to teach use of performance counters. Backer teaches a method of multiprocessor system running same operating systems on each node (see abstract). Backer also teaches a counter (fig. 1, items 26, 28 and 30), which keeps track of the shared memory accesses by each threads (column 3, lines 45-65). It would have been obvious to one having ordinary skill in the art at the time of the invention would have used the teachings of Backer to keep track of memory accesses using counters in the system of Harvey to determine utilization of the node by use of counters (Backer, column 2, lines 30-40) to allocate (replicate) frequently used memory in the respective nodes and thus improving system performance.

As per claim 4, Backer teaches an individual counter, which keeps track of memory accesses for individual node (fig. 1, column 3, lines 59-67 and column 4, lines 1-7). Backer fails to teach combining the counter value. It would have been obvious to one having ordinary skill in the art at the time of the invention would combined the all counter values to get total utilization of the whole system.

As per claims 5-7, Backer fails to teach keeping counter values for page allocations, disk accesses and look-aside list. It is well known that page table allocations; disk accesses and look-aside lists are parts of the memory accesses in the virtual memory addresses. It would have been obvious to one having ordinary skill in the art at the time of the invention would have used the counters for page allocations, disk accesses (kind of memory access) and look-aside lists to get precise utilization and to better allocate resources to individual nodes.

Claims 8-19 are also rejected under same rationale as applied to claims 1-7 above. The read/write variable as mentioned in the claims 8-10 are considered as counters from the description of the present application specification (page 5, paragraph [0015]).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Brock et al. (US 6,499,028 B1) and Schoinas et al. (US 6,347,362 B1) teaches a method of using counters in multiprocessor systems to keep track of shared memory accesses.

Nesheim et al. (5,897,664) teaches a multiprocessor system using virtual memory addressing and page tables.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is 571-272-5536. The examiner can normally be reached on 8.00 am - 4.30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kaushikkumar Patel
Examiner
Art Unit 2188

kmp

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER